AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An IC comprising[;]:

an internal circuit;

a debug I/F circuit for debugging the internal circuit from externally; and

an authentication circuit which is provided between the debug I/F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and authenticating from a reception signal received from the debug terminal and said transmission key to enable operation of the debug I/F circuit.

wherein said internal circuit comprises a CPU connected to said debug I/F circuit through a debug bus and a peripheral circuit connected to said CPU through an internal bus separated from said debug bus.

2. (Original) The IC according to claim 1, wherein the authentication circuit cancels a reset signal to the debug I/F circuit for enabling the operation.

3. (Currently Amended) The IC according to claim 1, wherein the authentication circuit generates an authentication key ~~that is encrypted~~ by encrypting the transmission key by a predetermined key, and collates said reception signal with the authentication key.

4. (Currently Amended) The IC according to claim 1, wherein the authentication circuit time-awaits the operation enabling after said authentication.

5. (Original) The IC according to claim 1, wherein the authentication circuit generates the transmission key by random numbers.

6. (Currently Amended) An electronic device mounted with an IC, said IC comprising[:]:

an internal circuit;

a debug I/F circuit for debugging the internal circuit ~~from~~ externally; and

an authentication circuit which is provided between the debug I /F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and collating ~~the~~ a reception signal received from the debug terminal with the transmission key to enable operation of the debug I/F circuit,

wherein said internal circuit comprises a CPU connected to said debug I/F circuit through a debug bus and a peripheral circuit connected to said CPU through an internal bus separated from said debug bus.

7. (Original) The electronic device according to claim 6, wherein the authentication circuit cancels the reset signal to the debug I/F circuit for enabling the operation.

8. (Currently Amended) The electronic device according to claim 6, wherein the authentication circuit generates ~~the~~ an authentication key ~~that is encrypted~~ by encrypting the transmission key by a predetermined key, and collates the reception signal with the authentication key.

9. (Currently Amended) The electronic device according to claim 6, wherein the authentication circuit time-awaits the operation enabling after said authentication.

10. (Currently Amended) The electronic device according to claim 6, wherein the authentication circuit forms the transmission key by the random numbers.

11. (Currently Amended) A debugging method for utilizing a debug I/F circuit and debugging an internal circuit from externally, comprising the steps of:

transmitting a transmission key to externally when the debug I/F circuit is activated; and

authenticating the a reception signal received from externally and the transmission key to enable operation of the debug I/F circuit,

wherein the step of authenticating further comprises connecting a CPU to said debug I/F circuit through a debug bus and connecting a peripheral circuit to said CPU through an internal bus separated from said debug bus.

12. (Original) The debugging method according to claim 11, wherein the authentication step includes a step of canceling a reset signal to the debug I/F circuit for enabling the operation.

13. (Currently Amended) The debugging method according to claim 11, wherein the authentication step includes[:]:

a step of generating [a] the authentication key ~~that is encrypted~~ by encrypting the transmission key by a predetermined key, and

a step of collating the ~~received~~ reception signal with the authentication key.

14. (Currently Amended) The debugging method according to claim 11, wherein the authentication step has a step of time-awaiting the operation enabling after said authentication.

15. (Currently Amended) The debugging method according to claim 11, wherein the transmission step has a step of forming the transmission key by the random numbers.

16. (Currently Amended) The debugging method according to claim 11, ~~wherein~~ further comprising[:]:

a step of receiving the transmission key and ~~encoding~~ encrypting the transmission key by a predetermined key, and transmitting the ~~received~~ reception signal with a discrimination device provided between a debugger and the debug I/F circuit.

17. (Currently Amended) A debugger for debugging an IC, the IC comprising an internal circuit; a debug I/F circuit for debugging the internal circuit; and an authentication circuit which is provided between the debug I/F circuit and the a debug terminal, said debugger comprising[:]:

a debug unit for debugging said ~~LSI~~ IC; and

a discrimination device which is provided between said debug unit and said debug I/F circuit, and for receiving a transmission key from said authentication circuit, encrypting said transmission key by a predetermined key, and transmitting the encrypted transmission key to said authentication circuit to enable debugging of said IC by said debug unit.

wherein said internal circuit comprises a CPU connected to said debug I/F circuit through a debug bus and a peripheral circuit connected to said CPU through an internal bus separated from said debug bus.